Specification Amendments

Please replace the corresponding original parts of the specification with the amended parts provided below.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to an analysis of a waveform for a telecommunication system or for a measurement equipment, and more particularly to a Digital Signal Processing of Multi-Sampled Phase (DSP MSP).
The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems and for a wide range of data rates and waveform timings.
The invention further includes Sequential Data Recovery from Multi Sampled Phase (SDR MSP), which is a version of the DSP MSP, which provides clock and data recovery for optical communications.

Background Art

~~Present waveform analyzers and serial data receivers use an analog front end for signal filtering, data recovery, and for a generation of data recovery sampling clock. Therefore more expensive bipolar or BICMOS technologies are needed to achieve sufficient performance, and said present designs have rather limited noise filtering capabilities and are able to cover only narrow application areas.~~
~~Analog design problems are further compounded by lower supply voltages which cause~~

~~insufficient voltage head room in deep sub-micron IC's which are becoming dominant in today's and future electronics.~~

~~There was a need for a waveform timing analyzer and a digital method of signal analysis which will reduce cost and complexity by replacing said analog or BICMOS technologies with less expensive CMOS technologies, and will improve noise filtering and increase programmability of data analysis algorithms and improve reliability of data recovery functions.~~

Background art for this invention is represented by the documents listed below:
D1 (PCT/CA01/00723 invented by Bogdan);
D2 (US 2002/0009171 invented by Ribo).

The D1 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits. However these D1 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing.
Therefore besides said high resolution phase capture, the D1 solution has fundamentally different principle of operation and produces entirely different results.
Consequently D1 can not contribute to any processing of much higher frequency signals commonly used in communication links.

The D2 solution represents latest generation of clock and data recovery (CDR) circuits which over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.
The D2 captures windows consisting of samples covering entire data bit interval.
Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.

Therefore the D2 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.
Obviously such window centering can only be achieved by phase locking to the received signal.
Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD). While taking more samples provides D2 with better base for jitter filtering than that of the CDR with BBPD, dynamics of D2 phase locking has to accommodate additional interference caused by said jiter filtering and by further processing of output data providing return reference for the D2 phase locked loop.

Similarly as the D2 and the CDR with BBPD, all other prior art analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to received signal in order to recover data based on sampling localized in a credible region of the received wave-form.
The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:

- Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.
- Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.
- Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of data links.

This invention is based on fundamentally different principle of operation and not only eliminates all the above deficiencies of the prior art but also has other significant advantages which are explained further below.
The major element of this invention is high resolution measurement of entire pulse lengths of incoming wave-form and digital processing of these accurate pulse lengths for determining

data content transmitted by the wave-form.

Since every edge detection provides exact re-timing of the whole received signal, such pulse lengths processing obviously never needs any phase locking.

Furthermore without any phase locking, based on an inexpensive local clock having frequency accuracy +/-30ppm, this invention provides phase jitter tolerance improvements over prior art which are listed below: over 6 times better tolerance in a lower 1/3 of received signal bandwidth, and 2 times better tolerance in the remaining upper 2/3.

Furthermore; since entire received wave-form is uniformly densely sampled and continuously filtered and processed, short glitches caused by high frequency amplitude noise are identified and filtered out before any detection of a valid edge takes place.

Since said exact re-timing is provided by every edge detection this invention solution locks instantly and never requires any acquisition time what makes it ideal for all the burst type ~~on~~ communication links.

JB Still other ~~over~~ major contributions over prior art include means for noise filtering based on advanced screening and analysis of captured over-sampled wave-forms and using noise filtering masks for adaptive noise filtering before any data error could occur.

The listed above and shown in the specification advantages shall be able to double transmission distance while reducing error rates at the same time.

The mentioned above improvements required multilevel contributing inventions such as; multiplying processing throughput with multistage sequential processing synchronized with high resolution high speed sampling circuits (SSP), multiplying speed and accuracy of arithmetic division needed to decode number of data entities in a received long pulse (FBS) etc..